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Date: June 18, 2004
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NOTICE OF SUBMISSION OF ARGUMENT

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Attorneys: Sang Ku Ha and Young Wook Ha

Korean Patent Application No.: 2002-0007454

Title of Inventions: Laminated Inductor

The present application is rejected on the grounds set below under Article 63 of the Korean Patent Law. If you have an argument or need an amendment, please submit an Argument or Amendment by the above deadline. The deadline can be extended by one-month each.

Ground

Claims 3 to 8 of the present application are not patentable under Article 29, Paragraph 2 of the Patent Law as follows.

1. The inventions described in claims 3 to 8 relate to an inductor which is stacked with coil patterns having a different number of turns. It is obvious over Fig. 2 and Fig. 4 cited invention (Japanese Patent Unexamined Publication No. 7-037719: Feb. 7, 1995).

[Enclosure] 1. Japanese Patent Unexamined Publication No. 7-037719 (February 7, 1995)

Dated June 18, 2004

Electric & Electronic Examination Bureau
Semiconductor Examination Division Examiner: In Chi Bok

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특허청 의견제출통지서

출원인	명칭 가부시키가이샤 무라타 세이사쿠쇼 (출원인코드: 519980960646) 주소 일본국 교토후 나가오카쿄시 덴진 2초메 26방 10고
대리인	성명 하상구 외 1명 주소 서울 서초구 반포1동 742-20 영화빌딩
출원번호	10-2002-0007454
발명의 명칭	적층인ектор

이 출원에 대한 심사결과 아래와 같은 거절이유가 있어 특허법 제63조의 규정에 의하여 이를 통지하오니 의견이 있거나 보정이 필요할 경우에는 상기 제출기일까지 의견서[특허법시행규칙 별지 제25호의2서식] 또는/및 보정서[특허법시행규칙 별지 제5호서식]를 제출하여 주시기 바랍니다. (상기 제출기일에 대하여 매회 1월 단위로 연장을 신청할 수 있으며, 이 신청에 대하여 별도의 기간연장 승인통지는 하지 않습니다.)

[이유]

이 출원의 특허청구범위 제 3-8 항에 기재된 발명은 그 출원전에 이 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 아래에 지적한 것에 의하여 용이하게 발명할 수 있는 것이므로 특허법 제29조제2항의 규정에 의하여 특허를 받을 수 없습니다.

1. 청구범위 제 3-8 항에 기재된 발명은 코일턴수가 서로 다른 코일패턴을 적층하여 구성된 인덕터에 관한 것으로 이는 인용에 일본국 특개평 07-037719('95.02.07)의 그림 2,4로부터 이 분야의 당업자가 용이하게 발명할 수 있는 것으로 인정됨.

[첨부]

첨부1 일본공개특허공보 평07-037719호(1995.02.07) 1부. 끝.

2004.06.18

특허청

전기전자심사국

반도체심사담당관실

-심사관 인치복



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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-037719
(43)Date of publication of application : 07.02.1995

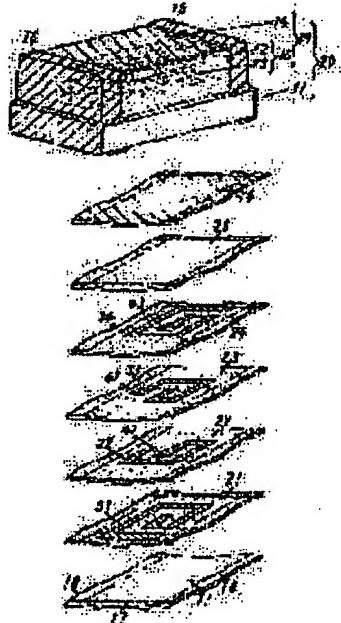
(51)Int.Cl. H01F 17/00

(54) CHIP INDUCTOR AND ITS MANUFACTURE

(57)Abstract:

PURPOSE: To flatten the top of a magnetic layer and contribute to high-density mounting by forming a shrinkage suppressing layer on the topmost layer of a laminating body and permitting the shrinkage suppressing layer to form a sintered layer before the magnetic layer is sintered.

CONSTITUTION: A bottom magnetic layer 21 is formed on one side of a sheet- shaped ceramic board 10 whereupon the primary separating groove 17 and the second separating groove 18 of a ceramic board 11 are processed. Then, a conducting layer 31, a magnetic layer 22 provided with a through hole and a conducting layer 32 are successively formed by printing permitting the conducting layer 32 to connect with the edge of the conducting layer 31 through the through hole. Such conducting layers and magnetic layers are alternately formed repeatedly for a prescribed number of conductor turns, and then a top magnetic layer 25 is formed. A shrinkage suppressing layer 14 formed of crystallized glass, magnetic material and low-softening point glass is formed by printing on a top magnetic layer 25. After baking the magnetic body, the conducting pattern and the shrinkage suppressing layer, formed on the ceramic board as a laminated body 19, the laminated body 19 is separated by the separating grooves 17 and 18 and edge plane electrodes are formed.



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[Date of request for examination]

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[Patent number]

[Date of registration]

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CLAIMS**[Claim(s)]**

[Claim 1] The inductor layer which consists of a conductor layer formed in said each magnetic layer so that it might connect with a lower layer conductor layer electrically through a heat-resistant insulating substrate, two or more magnetic layers which have SURUHORU or the excision section formed on this insulating substrate, said SURUHORU, or the excision section, The contraction control layer which consists of the quality of mixture or glass ceramics of a magnetic-substance ingredient and low softening temperature glass, is formed on said inductor layer, and controls contraction of said inductor layer at the time of baking, The chip inductor which consists of an end-face electrode of a pair which consists of said insulating substrate, said heat-resistant inductor layer, and heat-resistant contraction control layer, and which is really electrically connected with said conductor layer to the both ends of laminated material.

[Claim 2] The 1st process which forms a lower magnetic layer in a heat-resistant sheet-like insulating substrate, and forms the 1st conductor layer of 1 or more ****'s on said lower magnetic layer, Have SURUHORU or the excision section on said 1st conductor layer, and the 1st magnetic layer which thickness is 40-60 micrometers, and is twice [more than] the thickness of the 1st conductor layer is formed.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]**[0001]**

[Industrial Application] This invention relates to the chip inductor which carries out surface mounting to the high-density-assembly circuit board of small digital electronic equipment, and its manufacture approach.

[0002]

[Description of the Prior Art] In recent years, many chip inductors are used for the high-density-assembly circuit board accompanying small and thin-shape-sizing of a digital instrument as noise cure components etc.

[0003] Hereafter, the manufacture approach of the conventional chip inductor is explained. Drawing 5 is the perspective view showing the internal structure of the conventional chip inductor. Drawing 6 is the decomposition perspective view showing the manufacture approach of the conventional chip inductor.

[0004] Such a manufacture approach of the conventional chip inductor prints a magnetic layer 101, prints the conductor layer 201 of an abbreviation half turn on it, leaves the end of this conductor layer, prints a magnetic layer 102, and prints the conductor layer 202 of an abbreviation half turn on it further. After printing a magnetic layer 108 at the topmost part repeatedly and dividing into the piece of an individual until the predetermined number of turns is obtained in these processes, it calcinates, the end-face electrode 301 is formed, and a chip inductor is obtained.

[0005]

[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional configuration, it had the big trouble in respect of mass-production nature.

[0006] That is, since the laminating of the conductor layer of the pattern of an abbreviation half turn is printed and carried out in the manufacture approach of the conventional chip inductor, the number twice the count of conductor-layer printing of of coil turns is needed, and there are also that much many those connections. For this reason, the dependability of electrical installation became low as the number of turns at the time of a laminating increased, and it had the trouble that the yield at the time of mass production fell. Moreover, the thickness of a layered product increased to obtaining the coil of the number of high turns remarkably, and when there was a demand stored in a fixed dimension as a product, it had the trouble in the property side that a number of layers, i.e., an inductance value, is restricted.

[0007]

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TECHNICAL FIELD

[Industrial Application] This invention relates to the chip inductor which carries out surface mounting to the high-density-assembly circuit board of small digital electronic equipment, and its manufacture approach.

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PRIOR ART

[Description of the Prior Art] In recent years, many chip inductors are used for the high-density-assembly circuit board accompanying small and thin-shape-izing of a digital instrument as noise cure components etc.

[0003] Hereafter, the manufacture approach of the conventional chip inductor is explained. Drawing 5 is the perspective view showing the internal structure of the conventional chip inductor. Drawing 6 is the decomposition perspective view showing the manufacture approach of the conventional chip inductor.

[0004] Such a manufacture approach of the conventional chip inductor prints a magnetic layer 101, prints the conductor layer 201 of an abbreviation half turn on it, leaves the end of this conductor layer, prints a magnetic layer 102, and prints the conductor layer 202 of an abbreviation half turn on it further. After printing a magnetic layer 108 at the topmost part repeatedly and dividing into the piece of an individual until the predetermined number of turns is obtained in these processes, it calcinates, the end-face electrode 301 is formed, and a chip inductor is obtained.

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, by forming a contraction control layer in the maximum upper layer of a layered product, in order that a contraction control layer may form the sintering film previously before a magnetic layer sinters, this sintering film controls contraction of the upper part at the time of baking of the magnetic substance, and the chip inductor of this invention contributes to high density assembly by realizing flattening of the magnetic layer upper part. Furthermore, it becomes what whose dependability of the electrical installation between layers improved, and whose yield improved, and was excellent in the field of mass-production nature by the number of laminatings becoming fewer compared with the number of laminatings of the conventional chip inductor, a node's being abbreviation one half and ending, since the conductor pattern is formed further 1 or more ****s of hits, setting thickness of a magnetic layer to 40-60 micrometers in addition, and making thickness of a magnetic layer into twice [more than] conductor-layer thickness.

[0036] Moreover, when obtaining the same inductance, it becomes what was excellent also in the property side that a number of turns and a number of layers can be increased, and an inductance value can be expanded since total thickness became thin compared with the layered product thickness of the chip inductor of the former [become / fewer / the number of laminatings].

[0037] Moreover, there are no KAKE and crack of components at the time of mounting highly [anti-chip box reinforcement], since it is a ceramic substrate [finishing / sintering / moreover], dimensional accuracy is high and mounting nature is good, since the inductor is formed on the high ceramic substrate of a mechanical strength. Furthermore, since the magnetic layer is formed on a sheet-like ceramic substrate, like the corner guard mold thickness film chip resistor, manufacture is easy and rich in mass-production nature.

[0038] The chip inductor having the outstanding mounting nature by the advantage in the property side that the mass-production nature which was excellent in the conventional chip inductor with improvement in the yield which was not able to be realized from these things, and an inductance value are expandable, and flattening on the front face of a layered product is realizable.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional configuration, it had the big trouble in respect of mass-production nature.

[0006] That is, since the laminating of the conductor layer of the pattern of an abbreviation half turn is printed and carried out in the manufacture approach of the conventional chip inductor, the number twice the count of conductor-layer printing of coil turns is needed, and there are also that much many those connections. For this reason, the dependability of electrical installation became low as the number of turns at the time of a laminating increased, and it had the trouble that the yield at the time of mass production fell. Moreover, the thickness of a layered product increased to obtaining the coil of the number of high turns remarkably, and when there was a demand stored in a fixed dimension as a product, it had the trouble in the property side that a number of layers, i.e., an inductance value, is restricted.

[0007] It aims at offering the manufacture approach of a chip inductor to which the mass-production nature which this invention solves the above-mentioned conventional trouble, raised the yield of a product, and was excellent, and an inductance value are made to expand.

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MEANS

[Means for Solving the Problem] In order to attain this purpose, this invention is characterized by providing the following in a chip inductor. A heat-resistant insulating substrate. The inductor layer which consists of a conductor layer formed in said each magnetic layer so that it might connect with a lower layer conductor layer electrically through two or more magnetic layers which have SURUHORU or the excision section formed on this insulating substrate, said SURUHORU, or the excision section. The contraction control layer which consists of the quality of mixture or glass ceramics of a magnetic-substance ingredient and low softening temperature glass, is formed on said inductor layer, and controls contraction of said inductor layer at the time of baking. The end-face electrode of a pair which consists of said insulating substrate, said heat-resistant inductor layer, and heat-resistant contraction control layer and which is really electrically connected with said conductor layer to the both ends of laminated material.

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OPERATION

[Function] By this configuration, by forming a contraction control layer in the maximum upper layer of a layered product, in order that a contraction control layer may form the sintering film previously before a magnetic layer sinters, this sintering film controls contraction of the upper part at the time of baking of the magnetic substance, and the chip inductor of this invention contributes to high density assembly by realizing flattening of the magnetic layer upper part. [0010] Moreover, since the magnetic layer is formed on a sheet-like ceramic substrate, like the corner guard mold thickness film chip resistor, manufacture is easy and rich in mass-production nature. [0011] The chip inductor having the outstanding mounting nature by the advantage in the property side that the mass-production nature which was excellent in the conventional chip inductor from these things with improvement in the yield which was not able to be realized, and an inductance value are expandable, and flattening on the front face of a layered product can be offered.

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EXAMPLE

[Example] (Example 1) It explains hereafter, referring to a drawing about one example of this invention.
[0013] Drawing 1 is drawing showing the internal structure of the chip inductor in the 1st example of this invention. Drawing 2 is the decomposition perspective view of the chip inductor of the 1st example. the sheet-like ceramic substrate whose 10 is a heat-resistant insulating substrate in drawing 1 and drawing 2, the ceramic substrate into which 11 divided the sheet-like ceramic substrate 10, and 12 -- the magnetic substance and 13 -- an inner conductor and 14 -- a contraction control layer and 15 -- an inductor layer and 16 -- an end-face electrode and 17 -- a primary part groove and 18 -- a magnetic layer, and 31-34 show a conductor layer, and, as for a secondary part groove and 19, as for laminated material, and 21-25, a layered product and 20 really show SURUHORU, respectively, as for 41-43
[0014] The manufacture approach is explained using drawing about the chip inductor constituted as mentioned above.
[0015] first, one side of the sheet-like ceramic substrate 10 of the alumina system which processed the primary part groove 17 and the secondary part groove 18 so that it might become the ceramic substrate 11 on the corner guard whose piece of a piece after division is 2.0x1.25mm as shown in drawing 2 -- mostly, the magnetic-substance paste of a NiZnCu system is printed on the whole surface, it dries on it, and the lower magnetic layer 21 with a thickness of about 200 micrometers is formed.
[0016] Next, printing formation of the conductor layer 32 of 1 or more *****s is carried out at the thickness of about 20 micrometers so that printing formation of the magnetic layer 22 which has SURUHORU 41 for carrying out printing formation of the conductor layer 31 of the cut water of 1 or more *****s with the conductive paste of an Ag-Pd system at the thickness of about 20 micrometers, and connecting the edge of a conductor layer continuously is carried out with a magnetic-substance paste at the thickness of about 50 micrometers, and the edge of the lower conductor layer 31 may be continuously connected through SURUHORU 41.

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(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開平7-37719

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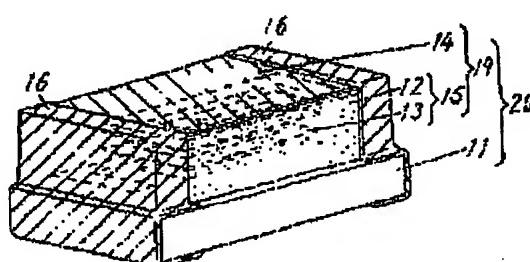
(54) 【発明の名称】 チップインダクタ及びその製造方法

(57) 【要約】

【目的】 デジタル機器の小型・薄型化に伴う高密度実装回路基板のチップ部品として、小型低背で実装性に優れかつ量産性に富んだチップインダクタの実現を目的とする。

【構成】 角板状のセラミック基板11と、スルホール41～43を有する逆性体層21～24とスルホール41～43を介して各々下層の導体パターンと電気的に接続する導体層31～34とからなるインダクタ層15と、結晶化ガラスと磁性体材料と低軟化点ガラスとかからなる収縮抑制層14とからなる。

- | | |
|------------|-----------|
| 11 セラミック基板 | 15 インダクタ層 |
| 12 逆性体層 | 16 端面導体 |
| 13 内部導体 | 17 精層体 |
| 14 収縮抑制層 | 20 一体積層物 |



(2)

特開平7-37719

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【特許請求の範囲】

【請求項1】 耐熱性の絶縁基板と、この絶縁基板上に形成されるスルホールまたは切除部を有する複数の磁性体層と前記スルホールまたは切除部を介して下層の導体層と電気的に接続するように前記各磁性体層に形成した導体層とからなるインダクタ層と、磁性体材料と低軟化点ガラスとの混合物質あるいは結晶化ガラスからなり前記インダクタ層上に形成され焼成時に前記インダクタ層の収縮を抑制する収縮抑制層と、前記耐熱性の絶縁基板および前記インダクタ層および収縮抑制層からなる一体積層物の両端部に前記導体層と電気的に接続する一対の端面電極とからなるチップインダクタ。

【請求項2】 シート状の耐熱性の絶縁基板に下部磁性体層を形成し前記下部磁性体層上に1ターン以上の第1の導体層を形成する第1の工程と、前記第1の導体層上にスルホールまたは切除部を有し厚さが4.0～6.0μmでかつ第1の導体層の厚さの2倍以上である第1の磁性体層を形成し、この第1の磁性体層上に厚さが前記第1の導体層と同様で1ターン以上あるいは1ターン未満の第2の導体層を前記スルホールまたは切除部を介して前記第1の導体層と接続するように形成する第2の工程と、前記第2の導体層上に上部磁性体層を形成し前記上部磁性体層上に収縮抑制層を形成する第3の工程と、前記各磁性体層および導体層からなるインダクタ層と前記収縮抑制層からなる積層体の端部に前記耐熱性の絶縁基板の上面から前記積層体を一部残して細分割用の溝を形成して接着した後前記あるいは構の隙に沿って前記積層体を一次分割して棒状の一體積層物を形成し前記一體積層物の両端部に端面電極を形成し前記あるいは溝の溝に沿って二次分割して複数のチップ状に細分割する第4の工程とからなり、前記第2の工程を所定の回数繰り返すことを特徴とするチップインダクタの製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は小型デジタル電子機器の高密度実装回路基板に面実装するチップインダクタ及びその製造方法に関するものである。

【0002】

【従来の技術】 近年、チップインダクタはノイズ対策部品などとしてデジタル機器の小型・薄型化に伴う高密度実装回路基板に多く使用されている。

【0003】 以下、従来のチップインダクタの製造方法について説明する。図5は従来のチップインダクタの内部構造を示す斜視図である。図6は従来のチップインダクタの側面構造を示す斜視図である。

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得られるまで繰り返し最上部に磁性体層108を印刷して個片に分割した後、焼成し、端面留置301を形成してチップインダクタを得るというものである。

【0005】

【発明が解決しようとする課題】 しかしながら、上記従来の構成では生産性の面で大きな問題点を有していた。

【0006】 すなわち、従来のチップインダクタの製造方法においては約半ターンのパターンの導体層を印刷し積層していくので、コイルターン数の2倍の導体層印刷回数を必要とし、その分それらの接続部も多い。このため積層時のターン数が多くなるにつれて電気的接続の信頼性は低くなり、積層時の歩留まりが低下するという問題点を有していた。また、高ターン数のコイルを得るために積層体の厚みが著しく増加し、製品として一定寸法内に収める要求がある場合、层数すなわちインダクタンス値が制限されるという特性面での問題点を有していた。

【0007】 本発明は上記従来の問題点を解決するもので、製品の歩留まりを向上させ優れた生産性ならびにインダクタンス値を拡大させるチップインダクタの製造方法を提供することを目的とする。

【0008】

【課題を解決するための手段】 この目的を達成するため本発明のチップインダクタは、耐熱性の絶縁基板と、この絶縁基板上に形成されるスルホールまたは切除部を有する複数の磁性体層と前記スルホールまたは切除部を介して下層の導体層と電気的に接続するように前記各磁性体層に形成した導体層とからなるインダクタ層と、磁性体材料と低軟化点ガラスとの混合物質あるいは結晶化ガラスからなり前記インダクタ層上に形成され焼成時に前記インダクタ層の収縮を抑制する収縮抑制層と、前記耐熱性の絶縁基板および前記インダクタ層および収縮抑制層からなる一体積層物の両端部に前記導体層と電気的に接続する一対の端面電極とからなるチップインダクタ。

【0009】

【作用】 この構成により、本発明のチップインダクタは積層体の最上層に収縮抑制層を形成することにより、磁性体層が焼成する前に収縮抑制層が先に焼成膜を形成するためこの焼成膜が磁性体の焼成時の上部の収縮を抑制し、磁性体層上部の平坦化を実現することにより高密度実装に寄与するものである。

【0010】 また、シート状のセラミック基板上に磁性体層を形成していることから角板型厚膜チップ抵抗器と同様に製造が容易で生産性に富んでいる。

【0011】 これらのことから、従来のチップインダクタの歩留まりを向上させ、生産性を高め、インダクタンス値を拡大するチップインダクタを提供する。

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て図面を参照しながら説明する。
【0013】図1は本発明の第1の実施例におけるチップインダクタの内部構造を示す図である。図2は第1の実施例のチップインダクタの分解斜視図である。図1、図2において10は耐熱性の絶縁基板であるシート状セラミック基板、11はシート状セラミック基板10を分割したセラミック基板、12は逆性体、13は内部導体、14は収縮抑制層、15はインダクタ巻、16は端面電極、17は一次分割溝、18は二次分割溝、19は銅層体、20は一体積層物、21～25は磁性体層、31～34は導体層、41～43はスルホールをそれぞれ示す。

【0014】以上のように構成されたチップインダクタについて図を用いてその製造方法を説明する。

【0015】まず、図2に示すように分割後の一個片が 2.0×1.25 mmの角板上のセラミック基板11になるように一次分割溝17および二次分割溝18を加工したアルミニナ系のシート状セラミック基板10の片面のほぼ全面にNiZnCu系の逆性体ベーストを印刷し乾燥して約 $200\mu m$ の厚みの下部逆性体層21を形成する。

【0016】次に1ターン以上の巻き始めの導体層31をAg-Pd系の導体ベーストで約 $20\mu m$ の厚みに印刷形成し、続いて導体層の端部を接続するためのスルホール41を有する逆性体層22を逆性体ベーストで約 $0\mu m$ の厚みに印刷形成し、続いて下の導体層31の端部をスルホール41を介して接続するように1ターン以上の導体層32を約 $20\mu m$ の厚みに印刷形成する。このように1ターン以上で約 $20\mu m$ の厚みの導体層とスルホールを有し約 $50\mu m$ の厚みの逆性体層を交互に繰り返し形成し、所定の導体ターン数になるまで繰り返す。この後、基板のほぼ全面を覆うように逆性体ベーストを印刷して約 $200\mu m$ の厚みの上部逆性体層25を形成する。

【0017】さらに前記上部逆性体層の上部に、結晶化ガラスと、逆性体材料50%と低軟化点ガラス50%を含む混合物質とからなる無機物質ベーストで収縮抑制層14を印刷形成する。これらセラミック基板上に形成された逆性体および導体パターンおよび収縮抑制層を積層体19とし、次にダイシング装置により溝幅を $200\mu m$ 以下にして積層体19をセラミック基板の上面から $100\mu m \sim 10\mu m$ の厚みを残してシート状セラミック基板の一次および二次分割溝に沿って溝加工する。これを $800^{\circ}C$ から $1100^{\circ}C$ の高温で1時間焼成する。

【0018】一方で、他の方法でアーチルの上に

【0019】(実施例2) 図3は本発明の第2の実施例におけるチップインダクタの内部構造を示す図である。図4は第2の実施例のチップインダクタの分解斜視図である。図3、図4において10は耐熱性の絶縁基板であるシート状セラミック基板、11はシート状セラミック基板10を分割したセラミック基板、12は逆性体、13は内部導体、14は収縮抑制層、15はインダクタ巻、16は端面電極、17は一次分割溝、18は二次分割溝、19は積層物、20は一体積層物、21～25は磁性体層、31～34は導体層、41～43はスルホールをそれぞれ示す。

【0020】以上のように構成されたチップインダクタについて図を用いてその製造方法を説明する。

【0021】図4に示すように分割後の一個片が 2.0×1.25 mmの角板上のセラミック基板11になるよう一次分割溝17および二次分割溝18を加工したアルミニナ系のシート状セラミック基板10の片面のほぼ全面にNiZnCu系の逆性体ベーストを印刷し乾燥して約 $200\mu m$ の厚みの下部逆性体層21とする。

【0022】次に1ターン以上の巻き始めの導体層31をAg-Pd系の導体ベーストで約 $20\mu m$ の厚みに印刷形成し、続いて導体層の端部を接続するためのスルホール41を有する逆性体層22を逆性体ベーストで約 $50\mu m$ の厚みに印刷形成し、続いて下の導体層31の端部をスルホール41を介して接続するように1ターン未満の導体層32を約 $20\mu m$ の厚みに印刷形成し、続いて導体層の端部を接続するためのスルホール42を有する逆性体層23を逆性体ベーストで約 $50\mu m$ の厚みに印刷形成し、続いて下の導体層32の端部をスルホール42を介して接続するように1ターン以上の導体層33を導体ベーストで約 $20\mu m$ の厚みに印刷形成し、続いて導体層の端部を接続するためのスルホール43を有する逆性体層24を逆性体ベーストを約 $50\mu m$ の厚みに印刷形成し、続いて下の導体層33の端部をスルホール43を介して接続するように1ターン未満の巻き終わりの導体層34を導体ベーストで約 $20\mu m$ の厚みに印刷形成する。この後、基板のほぼ全面を覆うように逆性体ベーストを印刷し約 $200\mu m$ の厚みの上部逆性体層25を形成する。

【0023】さらに前記上部逆性体層25の上部に結晶化ガラスからなる収縮抑制層14を印刷形成する。これらセラミック基板上に形成された逆性体層および導体層を積層体19とし、次にダイシング装置により溝幅を $200\mu m$ 以下にして積層体19をセラミック基板の上面から $100\mu m \sim 10\mu m$ の厚みを残して溝加工する。

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と接続する端面電極をA8系の厚膜導体を塗布したあと550°Cから900°Cで15分焼成することによって形成し、最後に二次分割焼成17に沿って分割し個片にしてチップインダクタを得る。

【0025】なお、各実施例において、セラミック基板を用いたがこれに限るものではなく、フェライト基板等の耐熱性の絶縁基板であればよい。また、各導体層の接続をする手段はスルホールに限定するものではなく、磁性体層の一部を切り欠く手段等、各導体層の接続を可能にするものであればよい。

* 【0026】このようにして得られた上部および下部磁性体層を除く中間の磁性体層が3層である場合の各実施例のチップインダクタの1kH₂におけるインダクタンス値、幅1.4mmの支持体の中央にチップインダクタを置きR0.5の加圧治具を使用してチップインダクタの中央部を加圧して破損したときの抗折強度およびチップ部品の実装率で1998個を実装したときの実装率を(表1)に示す。

【0027】

*10 【表1】

	収縮抑制層	特性		
		インダクタンス値 (nH)	抗折強度 (N)	実装率 (%)
実施例1	結晶化ガラス	912.6	10.3	100.00
	磁性体材料 +	965.3	9.4	99.95
	低軟化点ガラス			
実施例2	結晶化ガラス	580.9	10.6	29.95
比較例	なし	401.4	9.0	81.93

【0028】ここで(表1)に示す比較例は、約半ターンの導体層を繰り返し積層し収縮抑制層を形成しない従来のチップインダクタである。

【0029】この(表1)の結果から、本実施例1、2のチップインダクタは比較例のチップインダクタに比べてインダクタンス値が大きく、実装性もはるかに優れていることがわかる。

【0030】また本発明のチップインダクタおよびその

11上に導体パターンを内設した磁性体12上に形成された収縮抑制層14を設けることにより焼結時に発生する磁性体の反りを抑制し平坦化することができ、製品形状のばらつきが小さく実装性と量産性に優れたものができる。

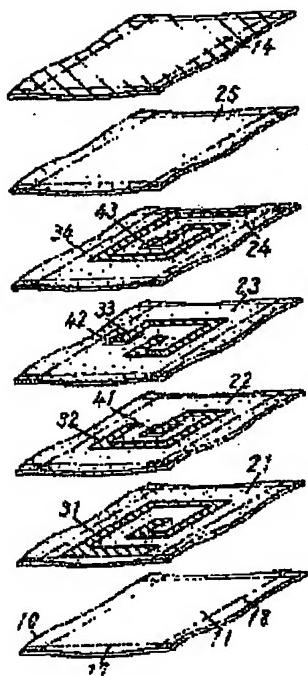
【0032】なお、上部および下部磁性体層を除く各導体層の厚みが40~60μmでかつ各導体層の厚みの2倍以上とした場合、磁性体層を挟んだ導体層間で短絡

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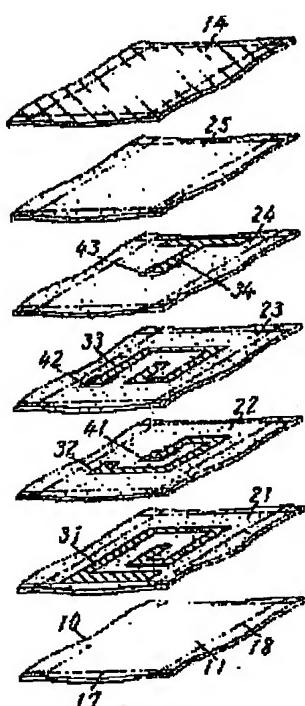
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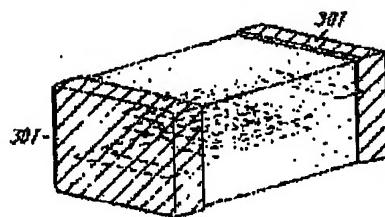
[圖2]



[圖4]



[図5]



[圖6]

